

**SSC8023GS6****P-Channel Enhancement Mode MOSFET****➤ Features**

VDS	VGS	RDSON Typ.	ID
-20V	±12V	65mR@-4V5	-3A
		90mR@-2V5	

**➤ Description**

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

**➤ Applications**

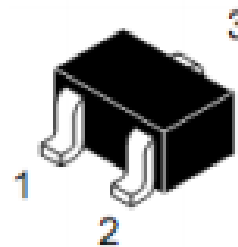
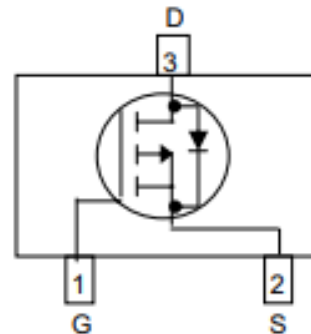
- Load Switch
- Portable Devices
- DCDC conversion

**➤ Ordering Information**

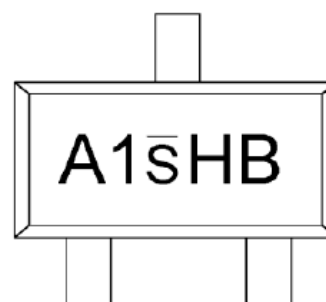
Device	Package	Shipping
SSC8023GS6	SOT-23	3000/Reel

**➤ Pin configuration**

Top view



SOT-23



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{\text{DSS}}$	Drain-to-Source Voltage	-20	V
$V_{\text{GSS}}$	Gate-to-Source Voltage	$\pm 12$	V
$I_{\text{D}}$	Continuous Drain Current <sup>a</sup>	-3	A
$I_{\text{DM}}$	Pulsed Drain Current <sup>b</sup>	-20	A
$P_{\text{D}}$	Power Dissipation <sup>c</sup>	0.8	W
$P_{\text{DSM}}$	Power Dissipation <sup>a</sup>	0.42	W
$T_{\text{J}}$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{\text{STG}}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta\text{JA}}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		300	$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JC}}$	Junction-to-Case Thermal Resistance		160	

Note:

- The value of  $R_{\theta\text{JA}}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_{\text{D}}$  is based on  $T_{\text{J(MAX)}}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

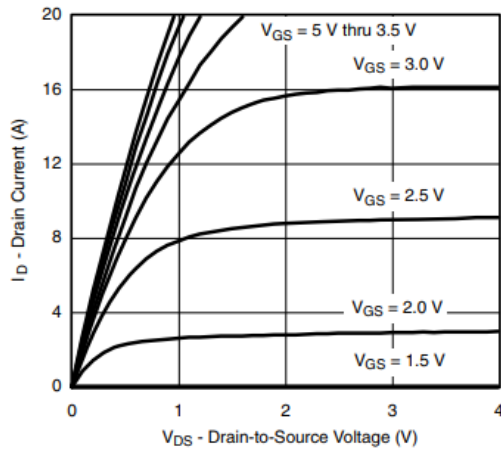


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

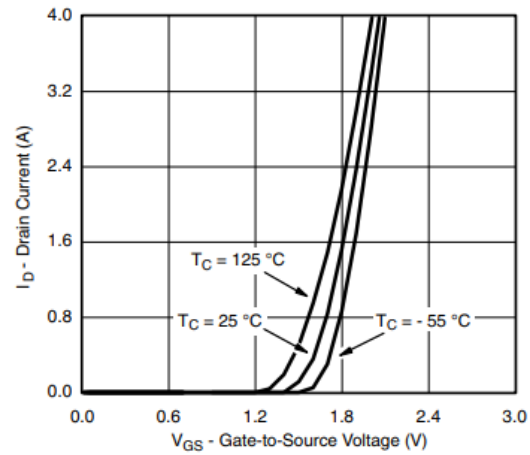
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu A$	-0.45	-0.75	-1.5	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-4.5V$ , $I_D=-2.8A$		65	90	mR
		$V_{GS}=-2.5V$ , $I_D=-2A$		90	140	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-20V$ , $V_{GS}=0V$			-1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V$ , $V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=-5V$ , $I_D=-2.8A$		6.5		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V$ , $I_S=-1.6A$	-0.5		-1.2	V
$C_{iss}$	Input Capacitance	$V_{DS}=-6V$ , $V_{GS}=0V$ , $f=1MHz$		415		pF
$C_{oss}$	Output Capacitance			223		
$C_{rss}$	Reverse Transfer Capacitance			87		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-6V$ , $V_{GEN}=-4.5V$ , $R_L=6R$ , $R_G=6R$ , $I_D=-1.0A$		13		ns
$T_r$	Rise time			10		
$T_{D(OFF)}$	Turn-off delay time			42		
$T_f$	Fall time			14		



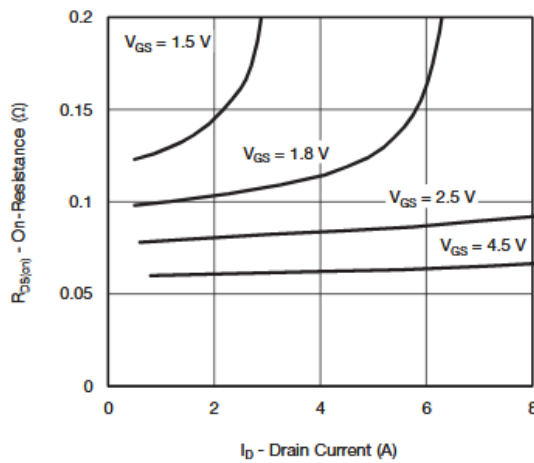
➤ **Typical Characteristics**( $T_A=25^\circ\text{C}$  unless otherwise noted)



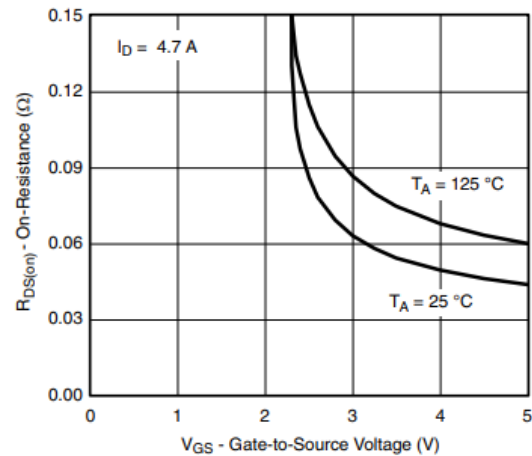
**Output Characteristics**



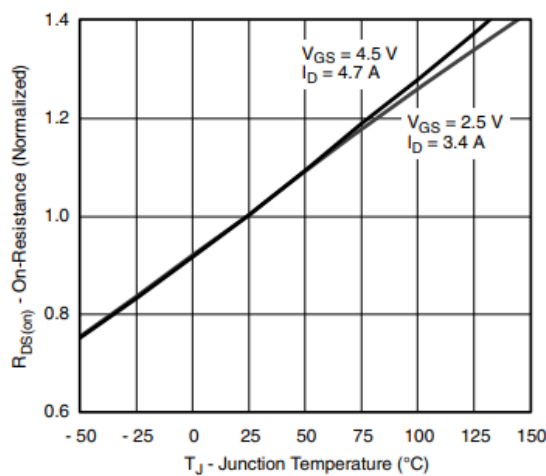
**Transfer Characteristics**



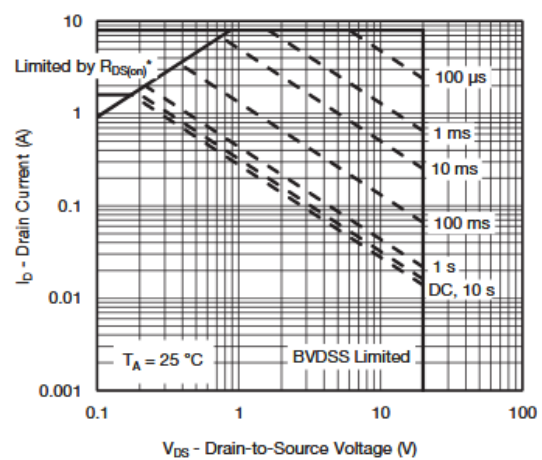
**On-Resistance vs. Drain Current**



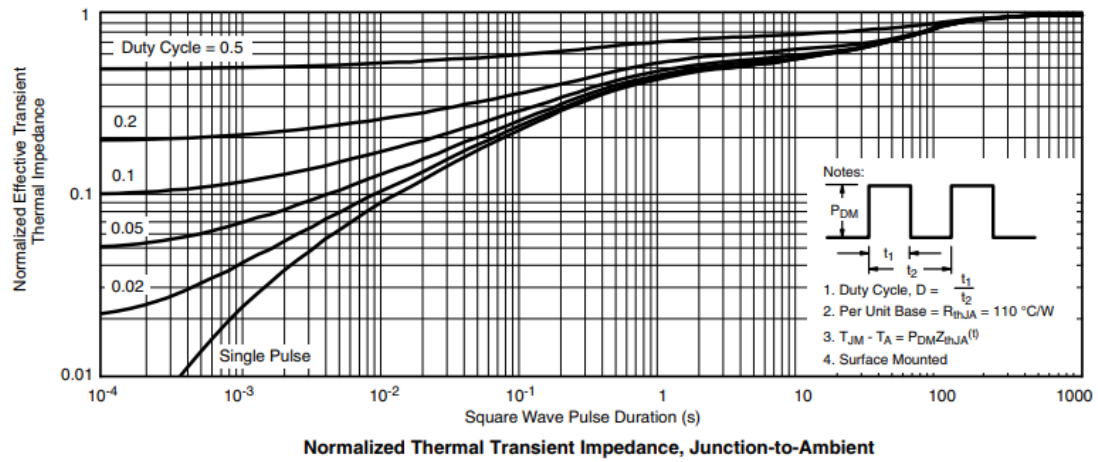
**On-Resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Junction Temperature**

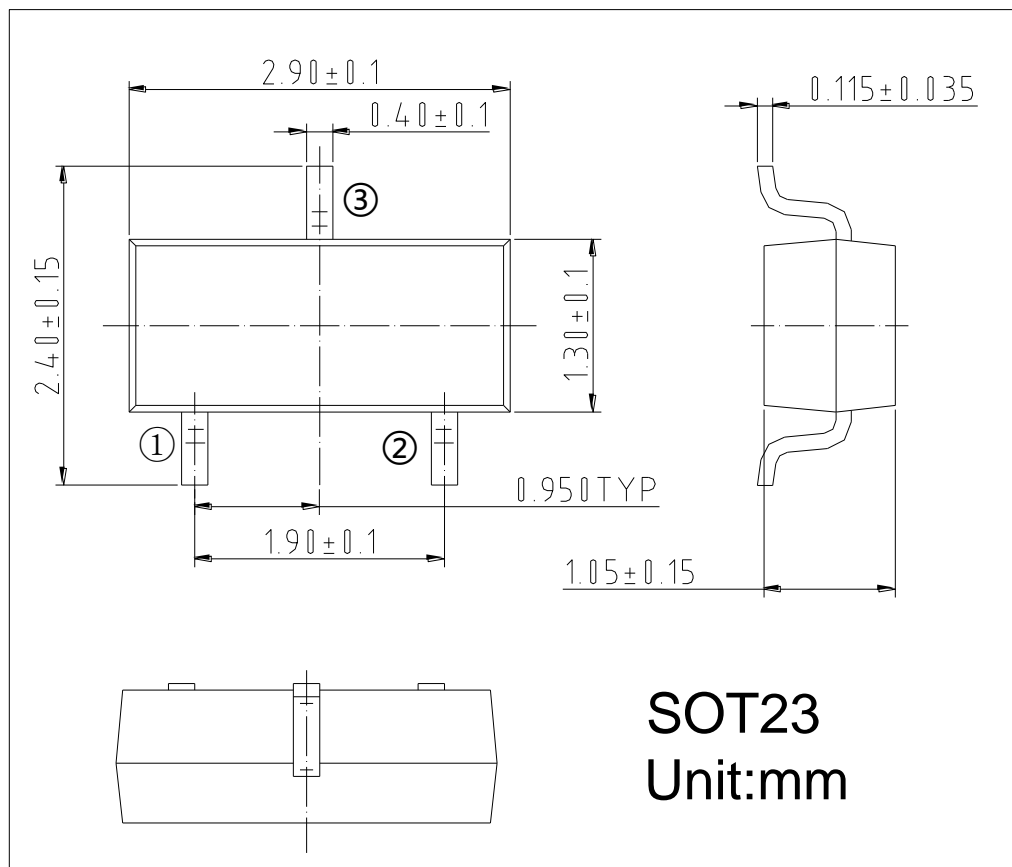


**Safe Operating Area, Junction-to-Ambient**

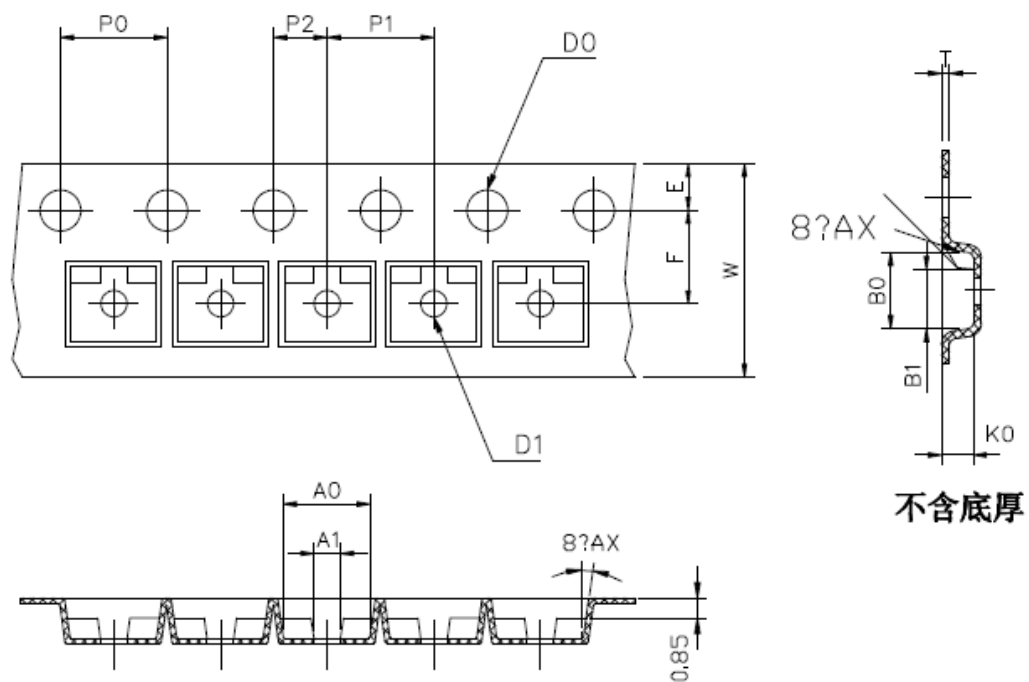




➤ Package Information



TAPE AND REEL DATA





## SSC8023GS6

Symbol	A0	A1	B0	B1	K0	D <sub>0</sub>	D <sub>1</sub>	P <sub>0</sub>	P <sub>1</sub>
Spec	3.15±0.10	1.15±0.10	2.80±0.10	2.15±0.10	1.30±0.10	1.55±0.10	1.10±0.10	4.00±0.10	4.00±0.10
Symbol	W	E	F	P <sub>2</sub>	t	t1	10*P0	4-P0	
Spec	7.95±0.05	1.70±0.05	3.50±0.10	2.00±0.10	0.21±0.02	0.05以上	40.00±0.10	4.00±0.10	

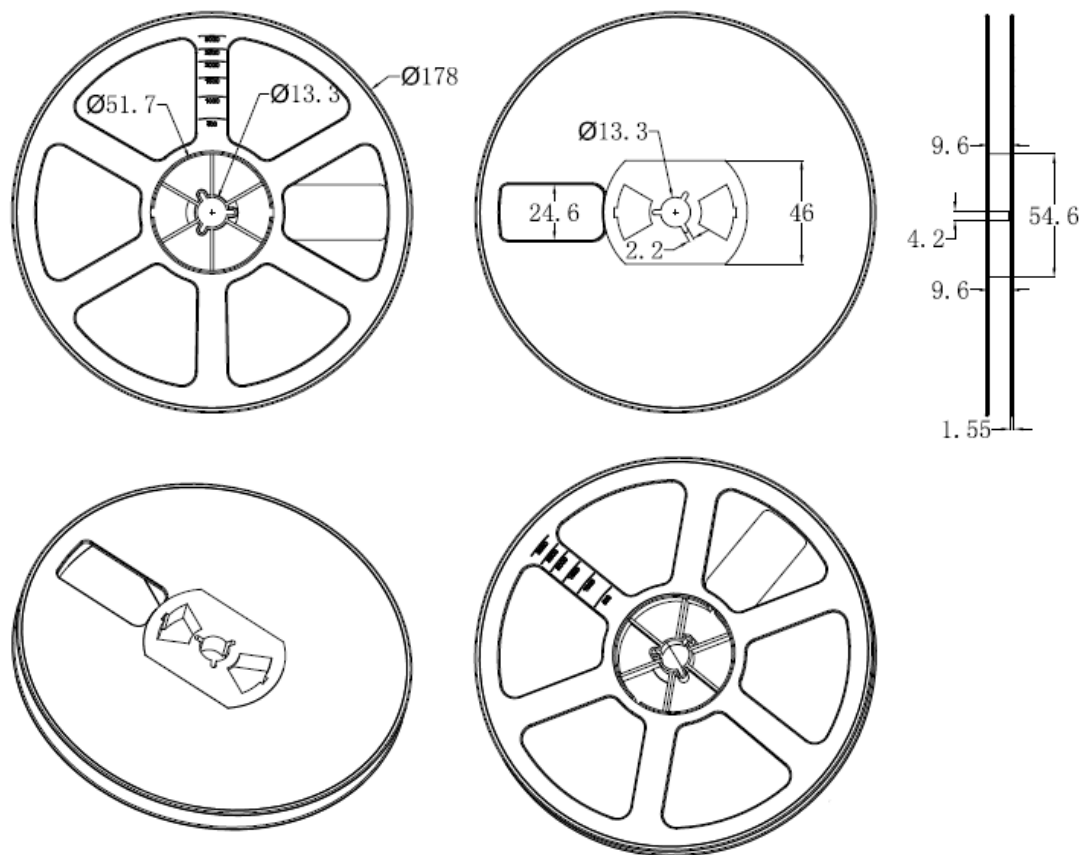
NOTE:

1.材料: PC+PS导电

2.10个链孔的累积公差不能超过0.2MM;

3.250MM带子的扇形不得超过1MM;

4.按照EIA-481-D的要求。





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